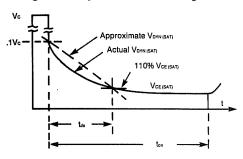


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Figure 2.15 - Dynamic Saturation Voltage.



Conduction losses, when it is necessary to account for dynamic saturation, can be approximated by the expression:

 $P_{ON} = [V_{CE(SAT)} * t_{on} + 1/2 * (0.1 * V_{CE(MAX)} - 1.1 * V_{CE(SAT)}) * t_{ds}] * I_{C(MAX)} * f Watts$

for ton greater than tds,

and

$$\begin{split} P_{ON} = & [0.1 * V_{CE(MAX)} - 1/2 * (0.1 * V_{CE(MAX)} - \\ & 1.1 * V_{CE(SAT)}) * t_{on}/t_{ds}] * I_{C(MAX)} * t_{on} * f \\ & Watts \end{split}$$

for ton less than tos.

where:

VCE(MAX) = Maximum Supply Voltage
VCE(SAT) = Transistor Saturation
(On State) Voltage
ton = Transistor on time
tds = Dynamic Saturation time
f = Switching Frequency

Since t_{ds} is so dependent on base drive and load conditions and typical values of t_{ds} are not a standard parameter shown on device data sheets, it is wise to determine t_{ds} by experimentally using your own base drive and load conditions.

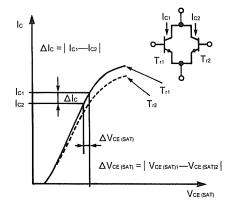
Parallel Operation

Operating Darlington transistors in parallel is an effective method to obtain higher operating currents than possible with a single module. When paralleling Darlington transistors, the total conducting time, i.e. the turn-on, turn-off and the on state must be considered for the paralleled transistors to share current equally.

In the on state, Darlington transistors tend to inherently share current due to the gain fall off at high currents preventing excessive current hogging by a single transistor and due to the negative feedback effect created by the increase in base to emitter voltage with an increase in collector current acting to reduce base current. The degree of static current sharing depends upon whether the transistors are operated in quasi saturation (V_{CE} greater than or equal to V_{BE}) or hard saturation (V_{CE} less than V_{BE}).

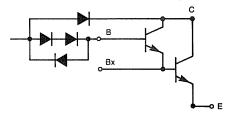
In quasi saturation operation, current sharing is determined by gain. Typical gain bands for Powerex Darlington transistors are illustrated in Figure 2.16. The Baker clamp, shown in Figure 2.17, is a very effective circuit to achieve quasi saturation operation and it is often used in parallel applications. It is usually sufficient to use a single series diode in the base lead instead of two as shown in Figure 2.17.

Figure 2.16 - Gain Matching and Typical Gain Bands For Darlington Transistors.



GAIN CLASS	h _{FE} RANGE
A	75 to 105
В	95 to 125
С	110 to 150
D	130 to 170
E	155 to 205
F	170 to 230
G	210 to 270
Н	245 to 315
J	280 to 360

Figure 2.17 - Baker Clamp Circuit.



Gain mismatch effects can be minimized by operating the transistors in hard saturation. When hard saturation operation is used it is not relevant to specify gain matching. For hard saturation operation, current sharing is determined by saturation resistance, and matching should be on $V_{\text{CE(SAT)}}$. Tests have shown that if transistors are overdriven into hard saturation, the $V_{\text{CE(SAT)}}$ can be matched to within 0.1 volt. A base current overdrive of two times the base current at minimum gain is necessary to achieve this overdrive.

With quasi saturation or hard saturation operation, VBE should be matched to eliminate any base current mismatch. Some articles recommend using individual base resistors for paralleled transistors fed from voltage sources significantly higher than $V_{\mbox{\footnotesize{BE}(SAT)}}.$ This and similar constant current drives are not recommended for paralleling Darlingtons because this type of base drive tends to oversaturate high gain transistors and leads to increasing the spread of storage time between the paralleled devices. Directly tieing the bases together of paralleled transistors causes the base current to divide among the transistors based upon gain. When VBE is matched, equal base currents will flow.



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Often, articles on paralleling transistors recommend using emitter resistors to force static current sharing. Emitter resistors work well in theory and in small signal applications. In high current Darlington applications, emitter resistors improve performance minimally at the expense of large power dissipation. Emitter resistors also increase the parasitic inductance in the emitter circuit which creates oscillation and dynamic sharing problems that are much worse than static mismatch. A similar recommendation is to use emitter inductors wound in opposition on a common core to provide static and dynamic current sharing. Again, in high current Darlington applications, emitter inductors create oscillation problems and usually deteriorate turn-off switching waveforms. Thus, emitter resistors and/or inductors are not recommended for paralleling high current Darlingtons.

The most critical aspect of paralleling Darlingtons is insuring dynamic current sharing. Turn-on sharing is generally not a problem if the bases are tied together and adequate base drive is provided. Turn-off sharing is the major problem area. The transistor with the longest storage time will be forced to turn off the entire load current which is most likely subjecting it to a turn off load line that is outside the device RBSOA limit.

At first glance it appears that one should match device storage times. But due to the large variation of storage time over temperature, it is not practical to match storage times. The best method to minimize storage time variations is to operate the devices in quasi saturation using an antisaturation circuit such as a Baker clamp. For paralleled Darlingtons, the Baker clamp circuit should be connected with individual series base diodes for each transistor and a single collector feedback diode for the entire paralleled set.

If the additional on state losses inherent in quasi saturation operation can not be tolerated and hard saturation operation is used, storage time differences can be minimized by high levels of I_{B2}.

Since high I_{B2} reduces RBSOA capability a turn off voltage snubber should be used to limit the collector to emitter voltage rise until after the collector current has reached a low value. The use of a turn off voltage snubber is recommended in all cases when paralleling Darlingtons because even if one transistor does end up turning off the entire load current the turn off snubber will prevent it from seeing high voltage when it is conducting high current.

Dynamic current sharing is also improved if the bases of the output transistors in the Darlington are connected together. Many Powerex Darlington transistors provide a Bx terminal which allows this connection. With the Bx terminals connected, the Darlington transistor which turns on first provides additional base current to the outputs of the remaining paralleled Darlingtons through the Bx connection, eliminating the delay in turn-on between the transistors.

The Bx connection also forces the transistors to share current during storage time, eliminating storage time differentials. The major portion of the storage time is in the input stage because the output stage is kept out of saturation by the Darlington connection. With the Bx terminals connected together none of the outputs begins to turn off until all of the input stages have turned off, making the transistors function as if the storage times were matched.

Although matching transistor parameters is important, subtle factors of base drive design and layout are more critical to successful paralleling of Darlington transistors. Devices must be mounted on a common heat sink in close thermal coupling with cooling applied evenly to maintain equal operating temperatures. Circuit layout should be such that emitter circuit inductance is minimized and symmetry. especially for power leads, is maximized. The drive circuit common should be connected to the common emitter terminals as close as possible to the packages to keep inductive and resistive drops in the high current wiring out of the drive circuit.

Due to their high gain, Darlingtons connected in parallel tend to develop parasitic high frequency oscillations. This is especially true when the bases of the paralleled devices are connected directly together as recommended above. High values of parasitic inductance in the emitter and base circuits and high levels of $l_{\rm B2}$ also tend to promote oscillation. These parasitic oscillations can often be eliminated by adding ferrite beads in the base leads. The series diodes of a Baker clamp circuit may also help to eliminate oscillations.